

ABSTRACT

A chip multiprocessor (CMP) includes a plurality of processors disposed on a peripheral region of a chip. Each processor has (a) a dual datapath for executing instructions, (b) a compiler controlled register file (RF), coupled to the dual datapath, for loading/storing operands of an instruction, and (c) a compiler controlled local memory (LM), a portion of the LM disposed to a left of the dual datapath and another portion of the LM disposed to a right of the dual datapath, for loading/storing operands of an instruction. The CMP also has a shared main memory disposed at a central region of the chip, a crossbar system for coupling the shared main memory to each of the processors, and a first-in-first-out (FIFO) system for transferring operands of an instruction among multiple processors.